forming n type impurity regions having a first concentration, for forming LDD regions of said n channel type TFT of said driving circuit and said pixel TFT in selected regions of said semiconductor islands;

forming n type impurity regions having a second concentration, for forming source regions or drain regions outside said LDD regions by introducing an n-type impurity thereinto while covering at least said LDD regions of said n channel type TFT of said driving circuit and said pixel TFT with resist masks, respectively;

forming a p type impurity region having a third concentration, for forming a source region or a drain region of said p channel type TFT of said driving circuit in a selected region of said semiconductor islands;

A1 Cont.

forming a protective insulation film comprising an inorganic insulating material over said n channel type TFT of said driving circuit, said pixel TFT and said p channel type TFT;

forming an inter-layer insulation film comprising an organic insulating material in close contact with said protective insulation film; and

forming over said inter-layer insulating film a pixel electrode having a light reflecting surface and connected to said pixel TFT.

30 (Amended). A method according to claim 29, wherein, as for said p channel type TFT of said driving circuit, the step of forming a p type impurity region having a third concentration, for forming a source region or a drain region of said p channel type TFT is conducted in a selected region of said semiconductor islands after said step of forming said protective insulation film comprising an inorganic insulating material, over the gate electrode of said p channel type TFT, and an offset region is formed between the channel formation region of said p channel type TFT and said

A1 p type impurity region having the third concentration, for forming the source region or the drain region.

Please add the following new claims:

53 (New). A method according to claim 31 wherein said low resistance conductive material comprises a material selected from the group consisting of Al and Cu.

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54 (New). A method according to claim 29 wherein said protective insulation film comprises a material selected from the group consisting of silicon oxide, silicon oxide nitride and silicon nitride.

55 (New). A method according to claim 29 wherein said protective insulation film has a thickness of 100 to 200 nm.

56 (New). A method according to claim 29 wherein said inter-layer insulation film has a mean thickness of 1.0 to 2.0 μm.

57 (New). A method according to claim 29 wherein said inter-layer insulation film comprises a material selected from the group consisting of polyimide, acryl, polyamide, polyimidamide and benzocyclobutene.

58 (New). A method according to claim 29 wherein said pixel electrode comprises a Ti film and an Al film.

59 (New). A method according to claim 29 wherein said p channel type TFT has a single drain structure.

60 (New). A method according to claim 29 wherein said LDD regions of said n channel type TFT of said driving circuit have a length of 1.0 to 4.0 μm.

A2

61 (New). A method according to claim 29 wherein said LDD regions of said n channel type TFT of said pixel TFT have a length of 0.5 to 4.0 μm.

62 (New). A method according to claim 29 wherein said semiconductor islands have a thickness of 25 to 80 μm.

63 (New). A method according to claim 29 wherein said driving circuit comprises a circuit selected from the group consisting of a shift register circuit, a level shifter circuit, a buffer circuit and sampling circuit.

REMARKS

Applicants will address each of the Examiner's rejections in the order in which they appear in the Office Action.

Claim Rejections - 35 USC §112

In the Office Action, the Examiner rejects Claims 29-33 under 35 USC §112, second paragraph as being indefinite. In particular, the Examiner objects to the phrase "island-like"